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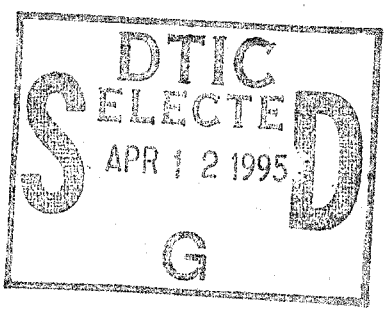

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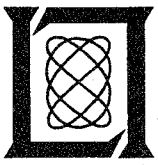

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The ESC Public Affairs Office has reviewed this report, and it is releasable to the National Technical Information Service, where it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

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SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

1 MAY — 31 JULY 1994

ISSUED 17 FEBRUARY 1995

LEXINGTON MASSACHUSETTS

ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 May through 31 July 1994. The topics covered are Electrooptical Devices, Quantum Electronics, Materials Research, Submicrometer Technology, High Speed Electronics, Microelectronics, and Analog Device Technology. Funding is provided primarily by the Air Force, with additional support provided by the Army, ARPA, Navy, BMDO, NASA, and NIST.

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INTRODUCTION

1. ELECTROOPTICAL DEVICES

An experimental optical analog link has been built for suboctave-bandwidth applications. This link has high dynamic range (>132 dB $Hz^{4/5}$), low detector photocurrent (0.94 mA), small noise figure penalty, and microwave frequency capability, and it is controlled with a single critical modulator adjustment.

2. QUANTUM ELECTRONICS

Radiation trapping has been shown to cause significant lengthening of the measured fluorescence lifetime in optically thin solid state laser gain media. This experimental artifact has led to underestimates of stimulated emission cross section by as much as 30% in Yb:YAG.

3. MATERIALS RESEARCH

A simple and inexpensive vertical gradient-freeze furnace has been used to grow 50-mm-diam, (111)-oriented InP crystals with dislocation densities in the range 10^3–10^4 cm^{-2}, compared to 10^4–10^5 cm^{-2} for crystals grown by the conventional liquid-encapsulated Czochralski method. The short-range doping uniformity is also much better for the crystals grown by the gradient-freeze method than by the Czochralski growth technique.

4. SUBMICROMETER TECHNOLOGY

Chemical mechanical polishing techniques have been developed to polish the back sides of silicon wafers, to planarize dielectric and resist layers, and to form self-aligned contacts. These techniques have been applied to the fabrication of imaging arrays, multichip modules, dense memory arrays, and Josephson junction devices.

A high-ion-density plasma etcher has been characterized for oxygen-based plasma development of a 193-nm silylation resist. Equal line and space gratings as small as 0.20 μm have been obtained with nearly vertical profiles and a large focus and exposure latitude.

5. HIGH SPEED ELECTRONICS

The effect of space charge on vacuum microtriode RF performance has been examined by numerical simulations using a finite element Poisson solver and particle trajectory code. For low work function emitters the space charge effects are adequately modeled by single tip calculations, but for high work function emitters the higher gate voltages cause the electron beams to flare substantially, so that the space-charge-limited current is determined by the entire array.

6. MICROELECTRONICS

The electron trapping properties of dislocations in CCDs have been determined using a technique that allows measurements of individual traps. A trap level 0.33 eV below the conduction band edge has been found, and this result explains the poor charge-transfer efficiency at low charge levels in devices with dislocations.

7. ANALOG DEVICE TECHNOLOGY

Experimental ferrite phase shifters have been demonstrated that utilize superconductor circuits with very low conduction losses. Differential phase shifters with meanderline circuits fabricated from niobium superconductors operated at 4 K have produced figures of merit exceeding 1000°/dB near 9 GHz, and the designs are adaptable to high-T_c superconductors.

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1 MAY THROUGH 31 JULY 1994

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Diode-Pumped Passively Q-Switched Picosecond Microchip Lasers	J. J. Zayhowski C. Dill III	*Opt. Lett.*

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Femtosecond Spectral Hole Burning in InGaAs/AlGaAs Strained-Layer Single-Quantum-Well Diode Lasers	C. K. Sun* B. Golubovic* H. K. Choi C. A. Wang G. D. Sanders* C. J. Stanton* J. G. Fujimoto*	9th International Meeting on Ultrafast Phenomena, Dana Point, California, 1-5 May 1994
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A Linearized Modulator for High Performance Bandpass Optical Analog Links	G. E. Betts	1994 IEEE MTT-S International Microwave Symposium, San Diego, California, 23-27 May 1994
Low-Loss Microwave Ferrite Phase Shifters with Superconducting Circuits	G. F. Dionne D. E. Oates D. H. Temme	
High-Power HTS Microstrip Filters for Wireless Communication	G.-C. Liang* D. Zhang* C. F. Shih R. S. Withers* M. E. Johanson* W. Rudy* B. F. Cole* M. Krivoruchko* D. E. Oates	

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Power Handling Capabilities of YBCO Films in Microwave Devices	D. E. Oates	
Three-Dimensional Servo System for 0.2-Micrometer-Resolution Laser Deposition and Etching	N. Nassuphis R. Mathews S. Palmacci D. J. Ehrlich	38th International Symposium on Electron, Ion and Photon Beams, New Orleans, Louisiana, 31 May–3 June 1994
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High Frequency Quantum Well Infrared Detector	H. C. Liu G. E. Jenkins E. R. Brown K. A. McIntosh K. B. Nichols M. J. Manfra	Device Research Conference, Boulder, Colorado, 20-22 June 1994
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193-nm Micrascan Update	M. S. Hibbs* R. R. Kunz	SPIE Lithography Working Group, Sunnyvale, California, 21 July 1994

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1. ELECTROOPTICAL DEVICES

1.1 OPTICAL ANALOG LINK USING A LINEARIZED MODULATOR

Many applications of external modulator optical analog links, such as antenna remoting and phased array antenna control, involve bandwidths of less than one octave. In these cases the modulator may be optimized without the constraint of minimizing second-order distortion. We have demonstrated a simple linearized modulator design that minimizes third-order distortion while providing a link noise figure as low as that of a link with a standard interferometric modulator, using the same input laser power. The average detector current (bias-point photocurrent) can be kept low to accommodate small-area microwave detectors and to minimize the effects of optical intensity noise.

The linearized modulator consists of two standard integrated optical Mach-Zehnder interferometric modulators (MZs) in series, as shown in Figure 1-1. (The device of Skeie and Johnson [1] is similar but minimizes both second- and third-order distortion by using reduced extinction on one modulator, which leads to more complexity and about a 6-dB noise figure penalty.) The RF input power is split between the two MZs to give the second MZ a modulation depth r compared to the first (the relative RF phase at the second modulator must be 0°). Three parameters control the modulator transfer function: r and the MZ phase bias points ϕ_1 and ϕ_2. We adjust these parameters to achieve minimum third-order distortion along with minimized detector current and low noise figure. The transfer function is independent of modulation frequency, and MZ modulators can be built at microwave frequencies, so this linearization technique is useful for high-speed applications. A more detailed theoretical description of this device can be found in Refs. 2 and 3; the focus here will be to present an experimental link built using this linearized modulator to illustrate the device's practicality and performance advantages.

The operation of this linearized modulator can be intuitively understood by considering the contributions to the cubic term of the modulator transfer function. The transfer function of the modulator is simply the product of the individual MZ responses. There is a contribution from the cubic term of each MZ individually,

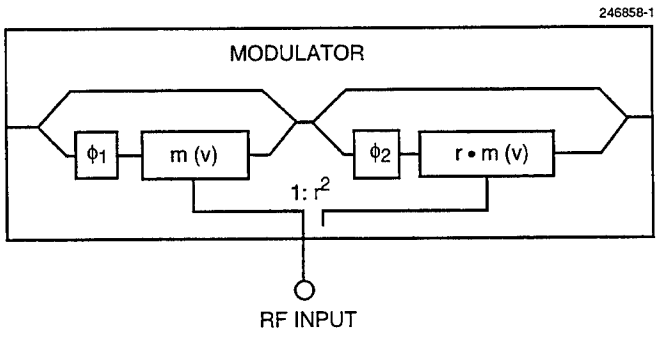

Figure 1-1. Series Mach-Zehnder interferometric modulator.

as well as from the product of the linear term of one modulator with the quadratic term of the other. The modulator parameters can be chosen so that, while the linear terms from the individual modulators add to maximize the fundamental, the product terms cancel the cubic terms from the individual modulators.

The experimental link is shown in Figure 1-2. In this demonstration r is set equal to 1 and ϕ_1 is set to ~ 90°. The bias point ϕ_2 (~ 118°) is actively controlled to minimize the third-order nonlinearity. The link was implemented with commercial components. The experimental link had ~ 11 dB of excess optical insertion loss: the 1320-nm, diode-pumped Nd:YAG laser launched 90 mW in the input fiber, the maximum detector current (both modulators at maximum transmission $\phi_1 = \phi_2 = 0°$) was 7.1 mA, and the responsivity of the 75-μm-diam InGaAs *pin* detector was 0.95 A/W. The average detector current at the operating point was only 0.94 mA. Though not fabricated for this demonstration, a monolithic series MZ device would reduce optical insertion loss and simplify packaging; for a monolithic device the excess optical loss would have been ~ 4 dB and the laser power for equivalent link performance would have been only 20 mW.

The results of a link test at 530 MHz are shown in Figure 1-3. A dynamic range of 88 dB was obtained with a 1-MHz noise bandwidth. As expected from theoretical calculations [3], the intermodulation distortion varies with a slope of 5 for large signals, with a local minimum just below the noise floor. If the bias point ϕ_2 were adjusted to maintain the slope of 5 for the intermodulation distortion down to small modulation depths, the dynamic range at the 1-MHz noise bandwidth would not be quite as large (82 dB), but the uniform behavior of third-order distortion with input power may be more practical. In this case the dynamic range normalized for noise bandwidth would be 132 dB $Hz^{4/5}$, with the units dB $Hz^{4/5}$ resulting from the slope of 5 for intermodulation distortion.

In addition to the small signal results, the large signal performance was investigated by using a single RF frequency. The maximum output signal power was approximately the same as could be achieved with a single MZ, which is expected since both reach 100% optical modulation depth. The output noise rises at large modulation depth because the average detector current rises (the dominant noise source in this link was shot noise), so the maximum signal-to-noise ratio achievable (161 dB Hz) was no better than for a single MZ.

The tolerances required to achieve this performance were reasonable, and the control method was simple; the theoretical tolerances for 3-dB dynamic range degradation were ± 1.0-dB ripple in RF power split, ± 10° in RF phase at the second MZ, and ± 0.15° in ϕ_2. The RF phase was set to 0° at all frequencies by simply adjusting the cable length to the second modulator so that the electrical signal arrived at the same time as light from the first modulator that had been modulated by that same signal (the power divider had less than ± 1.3° phase error over 10–1000 MHz). Errors in ϕ_1 and average r could be compensated by adjusting ϕ_2. The third-order distortion has a single minimum in the 0–180° range of ϕ_2, so control of that bias point was as easy as controlling the bias point of a single MZ for minimum second-order distortion.

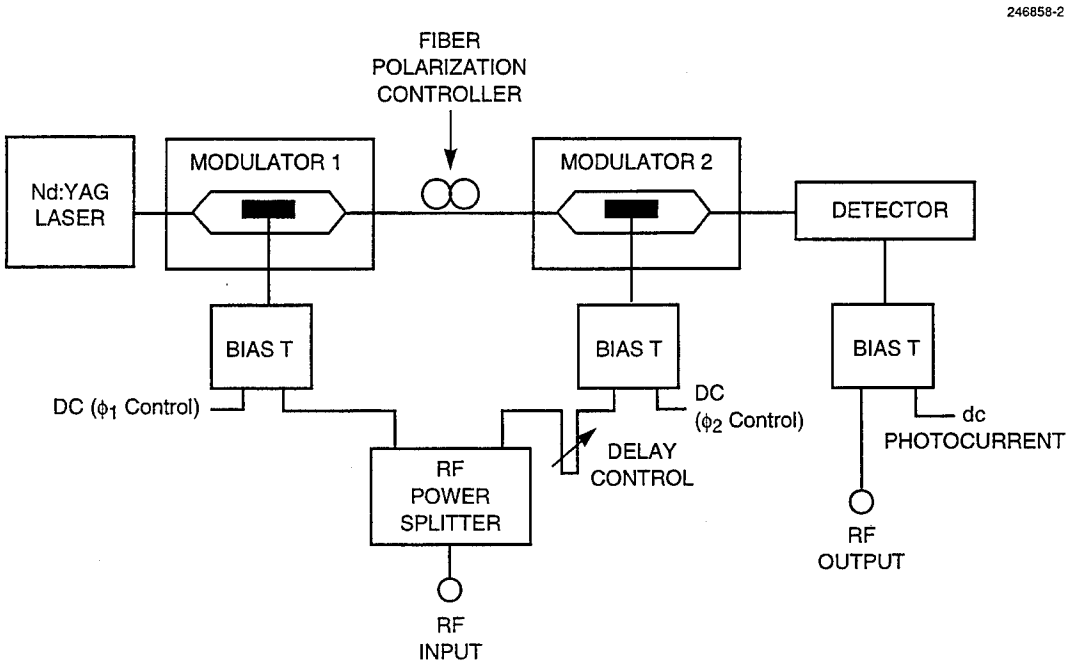

Figure 1-2. Block diagram of experimental link.

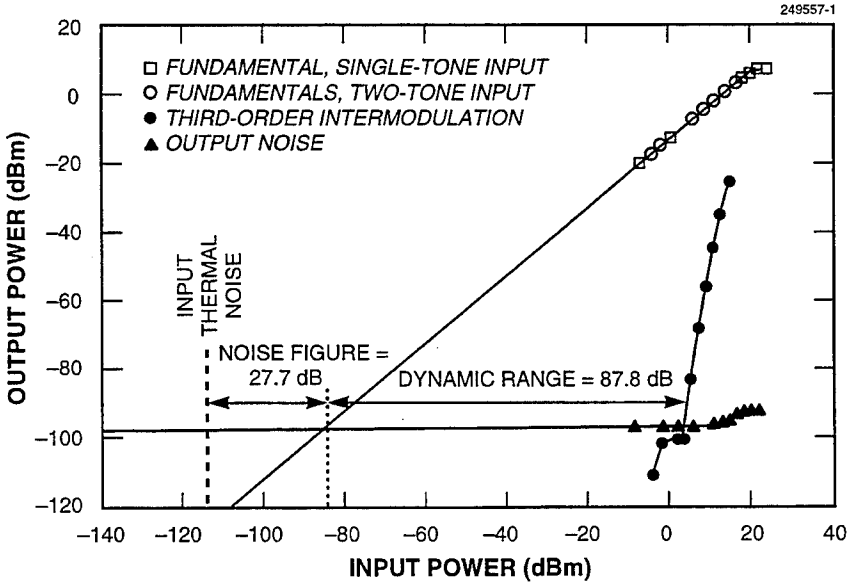

Figure 1-3. Measured performance of experimental link, with average detector current 0.94 mA, test frequencies 529 and 530 MHz, and noise bandwidth 1 MHz.

The performance of the series MZ link was compared with that of a link using a single MZ by setting the first modulator to maximum transmission and setting the second for the usual half-power bias (so $\phi_1 = 0°$ and $\phi_2 = 90°$), and applying all of the input RF power to the second modulator. Table 1-1 shows the results of this comparison. The electrical gain of the series MZ link is reduced, but the noise floor is lowered by approximately the same amount so the noise figure remains about the same. The third-order distortion is reduced, giving the series MZ link a much larger dynamic range.

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F. J. O'Donnell

TABLE 1-1

Comparison of Experimental Links Using Series MZ and Single MZ Modulators*

	Average Detector Current (mA)	RF Gain (dB)	Output Noise (dBm/Hz)	Noise Figure (dB)	Dynamic Range at 1 MHz† (dB)	Dynamic Range, Normalized‡
Single MZ	3.5	–4.5	–151.2	27.3	69.3	109.3 dB $Hz^{2/3}$
Series MZ	0.94	–10.8	–157.1	27.7	87.8	132 dB $Hz^{4/5}$
Change	—	–6.3	–5.9	+0.4	+18.5	—

*Maximum detector current is 7.1 mA for both.
†Maximum third-order intermodulation-free dynamic range obtained at 1-MHz noise bandwidth.
‡Dynamic range if bias point set for uniform fifth-degree intermodulation slope on series MZ.

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2. QUANTUM ELECTRONICS

2.1 IMPACT OF RADIATION TRAPPING ON FLUORESCENCE LIFETIME IN SOLID STATE LASER GAIN MEDIA

Three important spectroscopic emission parameters in solid state laser gain media are the stimulated emission cross section, metastable-level fluorescence lifetime, and metastable-level radiative lifetime. Accurate determination of these parameters is required for accurate laser modeling, but wide variations have been noted, particularly in the stimulated emission cross section. For example, measurements of the room-temperature effective stimulated emission cross section in Yb:YAG at 1.030 μm have ranged from 1.6 to 2.03 $\times$ 10^{-20} cm^2 [1]–[3]. The differences in the measured cross section can be explained almost entirely by differences in the assumed radiative lifetimes between the measurements. We have identified the primary source of error that leads to discrepancies in lifetime measurements, namely, radiation trapping.

In radiation trapping, photons that are emitted by spontaneous emission from the metastable level are "trapped" via reabsorption by ions in the ground state. These nascent excited-state ions then relax by emitting more photons, which are then reabsorbed. The net result is that the fluorescence lifetime, as measured over the volume of the sample, is increased relative to the lifetime of a single isolated ion. An accurate measurement of the true fluorescence lifetime is required in laser gain media in order to calculate the stimulated emission cross section, because the cross section is inversely proportional to the radiative lifetime, which is related to the fluorescence lifetime. Optically thin samples are typically employed in an attempt to eliminate radiation trapping [1],[4],[5]. If great care is not taken, however, radiation trapping can easily lead to overestimates in fluorescence lifetime of 30%, even in cases where optically thin media are used.

Yb:YAG was chosen as a prototypical system for quasi-three- and three-level lasers in which there is unity branching ratio of the fluorescence from the metastable level to the ground-state manifold. In these systems, radiation trapping is the most severe because of the large overlap of the fluorescence and absorption spectra. The fluorescence and absorption spectra of Yb:YAG at 300 K are shown in Figure 2-1. The fluorescence lifetime at 300 K has been variously measured using optically thin samples to be 1.08 [2], 1.16 [1], and 1.30 ms [4].

Optical thinness is an insufficient condition for eliminating radiation trapping effects because of total internal reflection (TIR) at the interface between a medium and air. Consider a medium that is optically thin in one dimension only, i.e., a thin plate. For YAG, with a refractive index of ~ 1.82, all spontaneous emission photons traveling at an angle > 33.3° with respect to the plate normal will experience TIR at the medium/air interface. This reflected emission increases the likelihood of reabsorption by neighboring ground-state ions. Radiation trapping increases with sample size, refractive index, and spectral overlap between fluorescence and absorption.

In order to eliminate radiation trapping to a larger degree, we used an optically thin plate of 5.5-at.%-doped Yb:YAG that was 3 $\times$ 5 $\times$ 0.2 mm in size. A YAG "sandwich" sample was formed by optically contacting the plate between two pieces of undoped YAG in the plane normal to the pump beam axis. The

optical contacting eliminates the TIR at the Yb:YAG/undoped-YAG interface and allows a larger fraction of the spontaneous emission to pass out of the sample and into the undoped region in a single pass before reabsorption can occur.

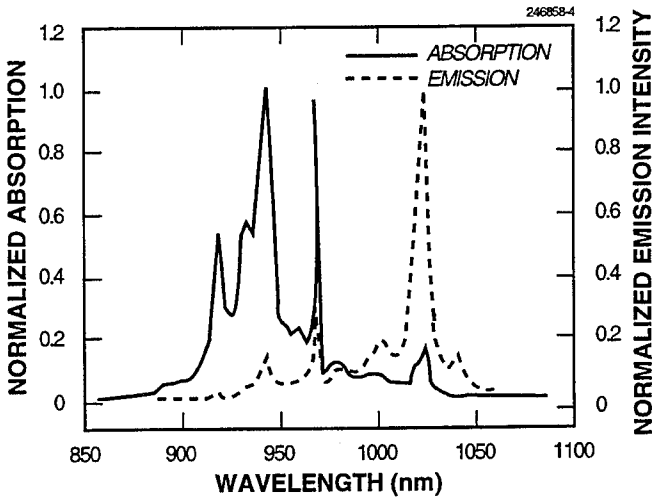

Figure 2-1. Normalized absorption and fluorescence spectra of Yb:YAG at 300 K.

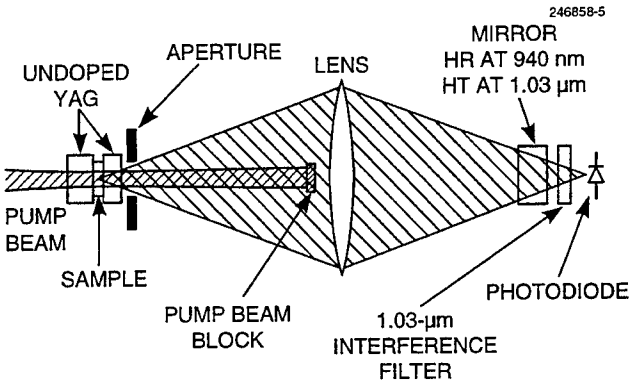

Figure 2-2. Schematic diagram of experimental fluorescence lifetime measurement. The Yb:YAG sample is optically contacted between two undoped YAG pieces to eliminate total internal reflection at the Yb:YAG faces.

A schematic of the experiment is shown in Figure 2-2. The pump beam at 940 nm was focused down to an ~ 0.5-mm-diam spot in the Yb:YAG sample to minimize the sample volume pumped and the fluorescence imaged onto a detector with a lens. Depending on the sample configuration and Yb^{3+} concentration, different-sized apertures were placed at the YAG sample to limit the transverse area of the sample seen by the detector, thereby reducing any signal from radiation trapped in the plane of the sample. The results are shown in Figure 2-3 for the 5.5-at.%-doped Yb:YAG sample as well as 1-, 10.8-, 16.5- and 25.1-at.%-doped samples prepared in a similar manner. Both 2.5- and 0.5-mm-diam apertures were used with the sandwiched samples. Figure 2-3 also shows measurements for unsandwiched samples in which a 2.5-mm-diam aperture was used, as well as Yb:YAG lifetime values from previous measurements. Based on the experimental results, the measured lifetime as a function of doping is constant for Yb^{3+} concentrations less than ~10 at.%, and therefore we can extrapolate a value for the fluorescence lifetime at zero concentration. In so doing, we have determined the radiative lifetime for the Yb:YAG $^2F_{5/2}$ manifold to be 951 μs ± 10 μs under the assumption that the radiative quantum efficiency is unity. The 1-at.%-doped sample was from the same boule used in Ref. 2 in which a 1.08-ms lifetime was measured, and the 5.5-at.%-doped sample is from the same boule in which the 1.16-ms lifetime was previously measured in Ref. 1.

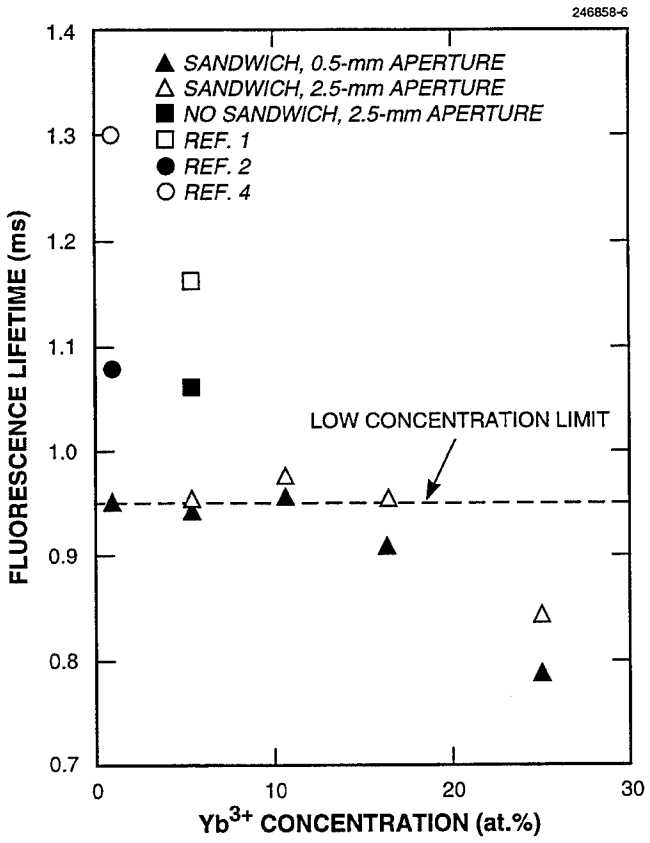

Figure 2-3. Measured fluorescence lifetime as function of Yb^{3+} concentration in Yb:YAG at 300 K for sandwich samples with various aperture sizes, unsandwiched samples, and previously reported values.

For the higher Yb^{3+} concentrations (above ~10 at.%), even the sandwiched configuration is insufficient for eliminating radiation trapping effects. However, by inserting a 0.5-mm-diam aperture to further limit the transverse area of the sample as viewed by the detector (effectively reducing optical thickness in the transverse dimension) a shorter lifetime was measured relative to using a larger 2.5-mm-diam aperture. The difference between these measurements is significant as the measured data points lie outside the error bars. Finally, we note that the measured lifetime decreased at higher Yb^{3+} concentrations. Concentration quenching is nonexistent in Yb^{3+}, in principle, and this observation is attributed to extrinsic concentration quenching due to trace impurities such as Tm^{3+}, Er^{3+}, and Cr^{3+}.

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*Author not at Lincoln Laboratory.

3. MATERIALS RESEARCH

3.1 VERTICAL GRADIENT-FREEZE GROWTH OF InP CRYSTALS

For a number of years InP crystals have been grown both with the liquid-encapsulated Czochralski (LEC) and the vertical gradient-freeze (VGF) methods. Figure 3-1 is a schematic diagram showing the LEC method, in which a seed is dipped into the melt and slowly pulled out under conditions that are adjusted to provide the desired diameter. Also shown in Figure 3-1 is the VGF method, in which the seed crystal is located in a well at the bottom of a melt that is frozen slowly from the seed upward as the temperature is decreased. In both cases, since the vapor pressure of P over molten InP is about 30 atm near the melting point, an encapsulating layer of B_2O_3 floats on the melt, which is contained in a vessel pressurized with argon to about 600 psi. Crystals grown by the VGF method invariably exhibit lower defect densities and better short-range doping uniformity than do those grown by the LEC method.

Because of the lower temperature gradients employed in the VGF method, particularly the radial gradients which provide very nearly planar horizontal isotherms, the crystal experiences much lower thermal hoop stresses during cooling. The density of dislocations, which are primarily generated by such stresses, is dramatically decreased from the typical 10^5–10^4 cm^{-2} for LEC crystals to 10^3–10^2 cm^{-3}. While dislocations do not appear to be an overwhelming problem for majority carrier devices or even for quaternary laser substrates, bipolar devices (especially solar cells) certainly should benefit from "dislocation-free" crystals.

Four (111)-oriented InP crystals grown by the VGF method are shown in Figure 3-2. To quantify the dislocation density, samples from such crystals are treated with a preferential etch using H_3PO_4 and HBr, and the etch pit density (EPD) is determined by counting in a 0.2-mm^2 area (in our case) under a microscope. Each etch pit corresponds to the intersection of a dislocation with the sample surface. Figure 3-3(a) shows EPDs as a function of distance along the diameter for (111) wafers cut from two undoped VGF single crystals. A similar plot is shown in Figure 3-3(b) for a smaller-diameter, undoped LEC crystal exhibiting much higher dislocation density. The W-shape is a result of high tensile stress near the periphery, compressive stress at the center, and an annular transition region in between, all created by thermal contraction during cooling in the high-temperature gradients. The dislocation densities in the VGF crystal are clearly lower than those in LEC crystals and show no strong hoop stress patterns.

Because of the stabilizing temperature gradient in the VGF method with cooler seed at the bottom of the melt, compared to the destabilizing LEC gradient with the seed at the top, buoyancy-driven convection currents in the VGF melt are minimized. Therefore, growth striations, consisting of spatial variations in doping concentration caused by changes in the boundary layer induced by the convection, are for the most part absent in VGF crystals. The doping concentration in LEC material can change, at worst, by nearly an order of magnitude over a 50-μm longitudinal distance across a striation. At best, with rapid rotation to stir the melt or with a magnetic field to damp the convection, it still generally varies by a few percent. Growth striations in LEC crystals are easy to observe and are sometimes viewable with the naked eye on a chemically etched surface. By contrast, the short-range doping uniformity is so good in VGF boules that the striations are not visible, even when searching for signs of the solid-liquid growth interface shape over the entire length of the boule in longitudinal slices with infrared transmission photography or x-ray topography. Only at the seed-on point can the interface shape be determined.

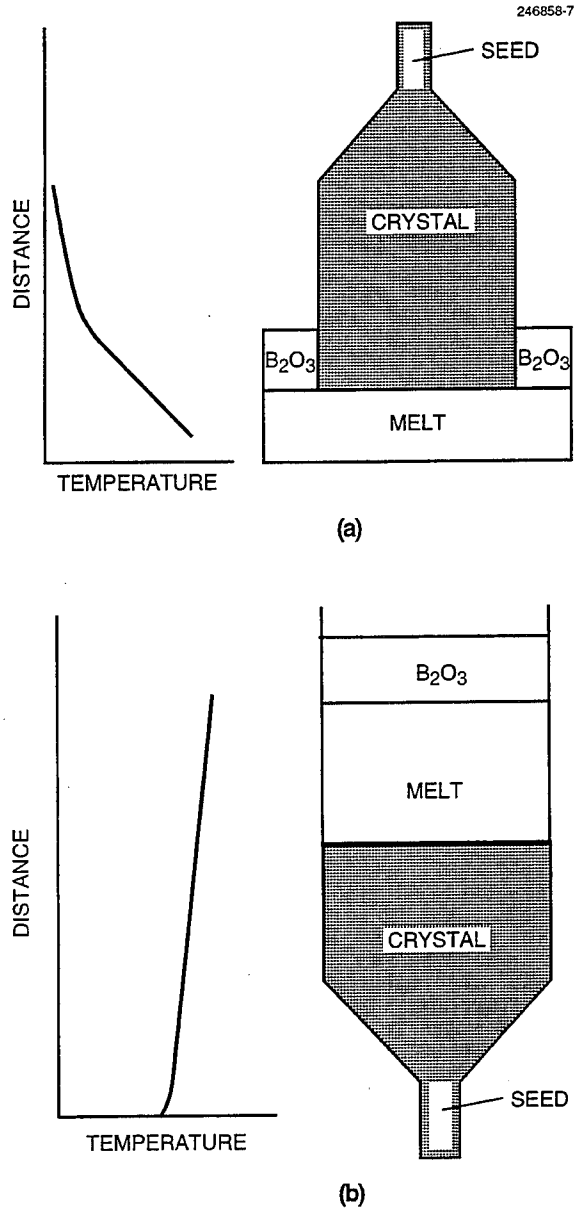

Figure 3-1. InP crystal growth by (a) liquid-encapsulated Czochralski (LEC) method and (b) vertical gradient-freeze (VGF) method.

The low defect densities that we observe in these crystals are in complete agreement with the earlier results of Monberg et al. [1]. Their VGF technique, however, unlike ours, incorporated crystal rotation during growth. Therefore, presumably because of slightly imperfect radial temperature uniformity, rotation striations were clearly seen in their infrared transmission photographs of longitudinal sample slices. These authors did not report the extent of the variation in doping concentration across the striations.

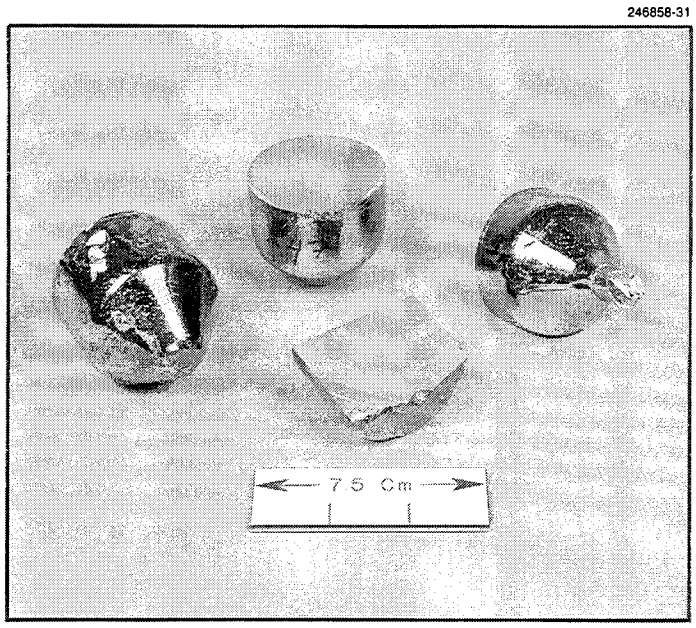

Figure 3-2. Four InP boules grown by VGF method. Several twins are noticeable in the center front boule.

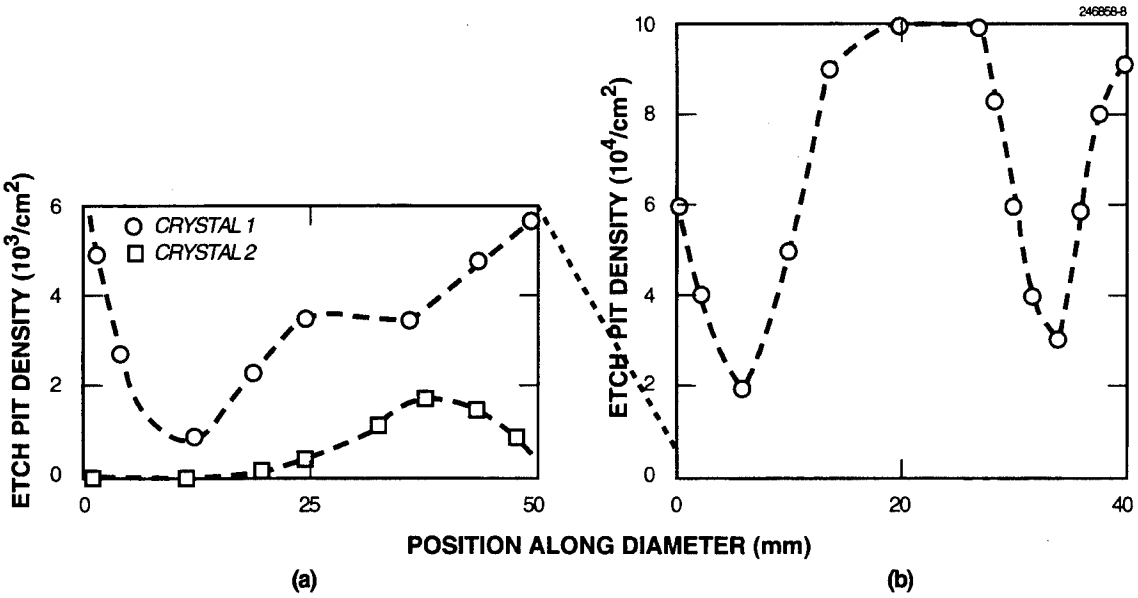

Figure 3-3. Etch pit density as function of position along diameter of (111) InP wafers from crystals grown by (a) VGF method and (b) LEC method.

Despite the better defect density and short-range doping uniformity of VGF crystals compared to LEC material, the measured electrical properties are not noticeably different. Thus, undoped VGF crystals exhibit electron concentrations in the low-10^{15}-cm^{-3} range, and the resistivities of semi-insulating Fe-doped crystals are generally between 10^7 and 10^8 Ω cm with 2000–3000-cm^2 V^{-1} s^{-1} mobilities. In photorefractive two-beam, 1.06-μm mixing experiments [2], the best dimensionless gain was obtained in a VGF crystal, perhaps because of the better uniformity of the Fe concentration or because the compensation ratio happened to be optimized.

Twinning remains a problem for VGF growth in an ampoule with a small-diameter seed and a conical section like that shown in Figure 3-1. While a high yield of single-crystal (111) growth has been achieved in such ampoules, the conical section tends to promote twinning for (100) growth. We have therefore begun to experiment with flat-bottom growth ampoules of constant diameter. Although we have not yet succeeded in single-crystal (100) growth because of a number of failed control thermocouples, a water shutdown, and a heater burnout, we have obtained initial growth without twinning. Recently, Matsumoto et al. [3] reported 50-mm-diam single-crystal (100) growth in flat-bottom crucibles. By employing a VGF growth furnace with pyrolytic graphite plates on a water-cooled base, as shown schematically in Figure 3-4, we have been able to

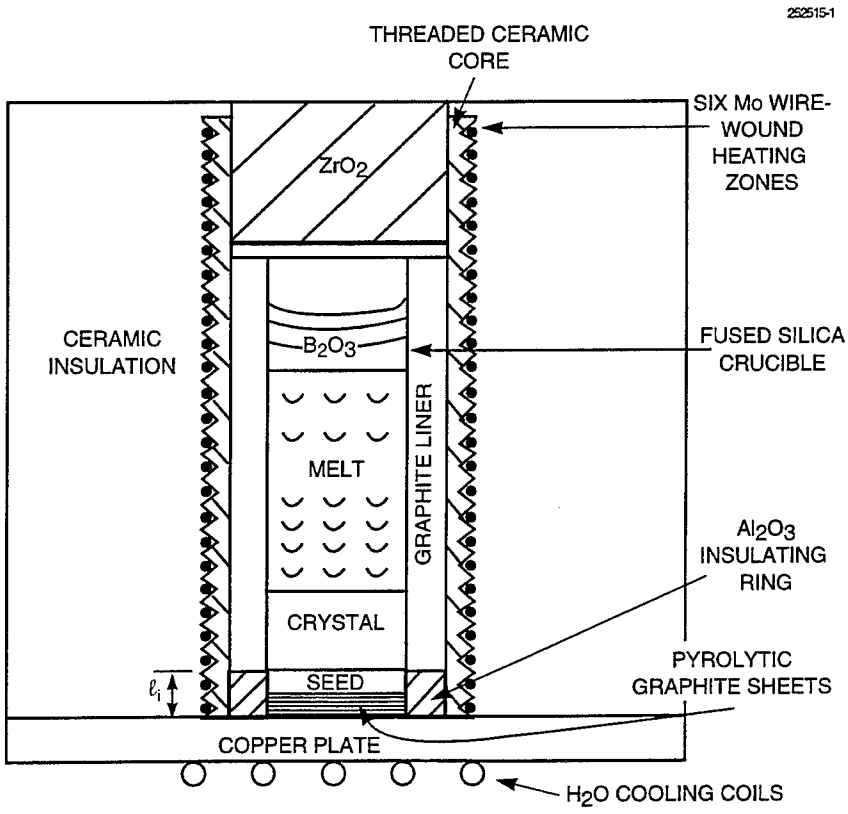

Figure 3-4. Schematic cross section of flat-bottom VGF crystal growth apparatus.

vary the solid-liquid shape at the seed-on point from concave to planar to convex, by changing the relative power supplied to the six heating zones and the length ℓ_i of the lower insulator. Our VGF system is a relatively simple growth station that can be assembled in the laboratory from the component parts (including the Mo wire) in a short time, and probably at less than 10% of the cost of the conventional multizone dynamic-gradient furnace employed for the VGF growth of GaAs. A typical temperature profile measured near the centerline of the furnace is shown in Figure 3-5, which was obtained by dipping a thin-wall closed-end fused silica tube containing a thermocouple through the B_2O_3 directly into the InP melt. The maximum vertical gradient is ~ 20°C cm^{-1}, compared to the hundreds of degrees per centimeter typically found in high-pressure LEC growth.

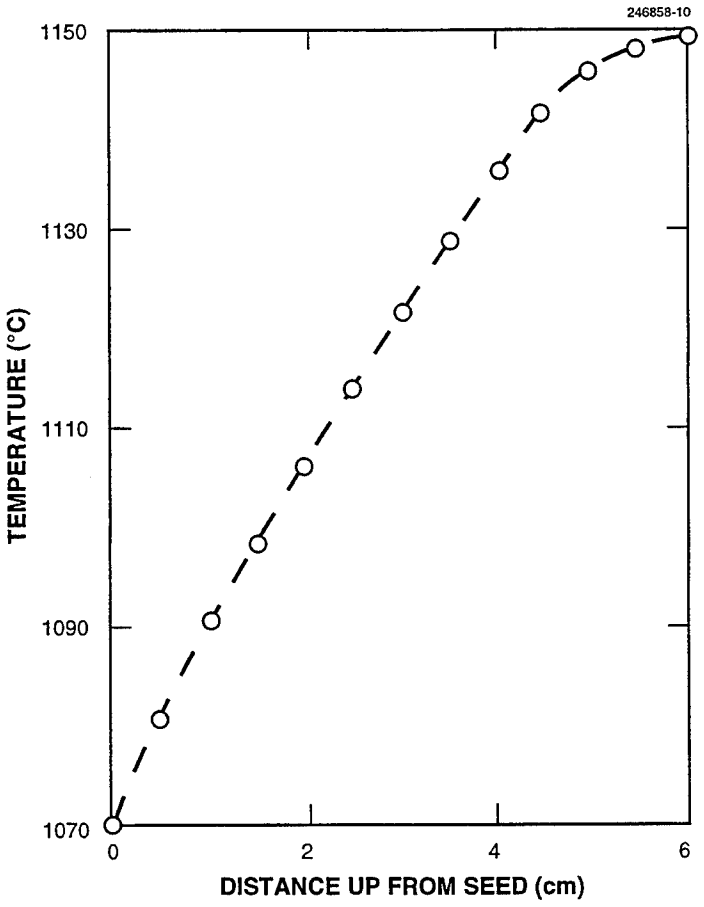

Figure 3-5. Temperature profile measured inside InP VGF melt just prior to crystal growth.

In addition to the limitation of yield of (100) single crystals because of twinning, a second problem remains for InP crystal growth. Notwithstanding the good short-range uniformity, the overall variation in doping concentration along the entire length of the VGF boule is still very large, since the segregation coefficients of almost all of the dopants used for InP are far less than unity. For example, the first-to-freeze part of an Fe- or Sn-doped boule contains only about 50% doping concentration at the center of the boule, 25% concentration at the point where 75% of the crystal has been grown, and 10% concentration where 90% has been frozen.

In an attempt to improve both the long-range segregation and the twinning problems, we have begun to experiment with a submerged heater in the InP melt, which is housed in a separate fused silica container. As shown in Figure 3-6, the submerged heater container fits closely inside the constant-diameter VGF crucible to provide a nearly planar isotherm just above the crystal/melt interface. Since it has been shown that a high twinning probability is closely related to nonplanar interface shapes in LEC growth of GaAs [4], we believe that the submerged heater may also decrease the twinning probability in the VGF growth of (100)-oriented InP. If the annular space between the heater container and the crucible wall is small enough to prevent the melt below the heater from mixing with the melt above it, it should also be possible to dope VGF crystals uniformly from bottom to top. For example, if a semi-insulating crystal that is uniformly doped with Fe at ~ 10^{16} cm^{-3} from top to bottom is desired, Fe would be charged into the region just below the submerged heater to provide a concentration of ~ 10^{19} cm^{-3} in that region, since only ~ 10^{-3} of the Fe in the melt is incorporated into the crystal. Either undoped or normal Fe-doped materials could be used above the heater. To the extent that the submerged heater is raised at the proper rate to keep the volume of liquid below it constant, and that none of the Fe is mixed into the melt above the heater, the VGF crystal should contain a constant Fe content.

Two test runs have been made to date with the submerged heater, one to attempt crystal growth and one specially designed to estimate the ratio of the thermal conductivity of the liquid k_l to that of the solid k_s. The first run was not successful in achieving single-crystal growth because the charge melted down from the top to within only ~ 1 mm of the seed and very small-grained polycrystalline growth resulted. In the second run, a small-diameter thermocouple was added well down through the center of the heater and into the charge below, the entire charge was melted, about half of it was frozen, and the axial temperature gradient in the melt was compared to that in the solid. The estimate that was obtained for k_l/k_s was ~ 1.8, and more work is in progress to obtain a better estimate for this ratio.

G. W. Iseler

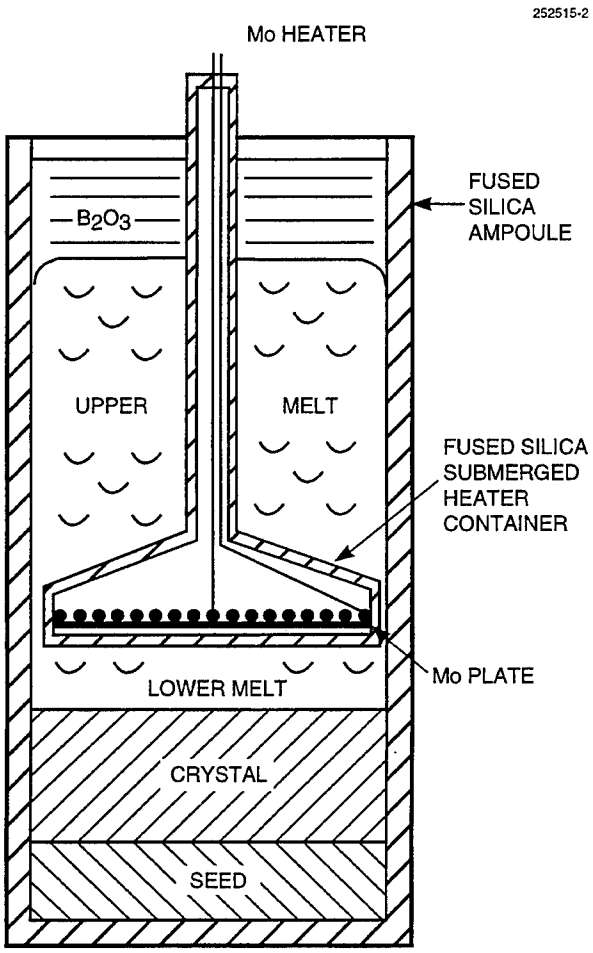

Figure 3-6. Schematic cross section of flat-bottom VGF crystal growth apparatus with submerged heater.

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4. SUBMICROMETER TECHNOLOGY

4.1 APPLICATIONS OF CHEMICAL MECHANICAL POLISHING

Chemical mechanical polishing (CMP) of silicon wafers prior to device fabrication has been used for many years to produce high-quality starting material for integrated circuit (IC) manufacturing. Recently, however, CMP is finding an increasing number of applications in the IC manufacturing process itself. Several IC manufacturers (IBM, Intel, and Motorola) have already implemented CMP for planarizing intermetal dielectrics used in their advanced multilevel metallization processes, and many other companies have active research programs in CMP [1]. The CMP technology alleviates two important problems faced by advanced metallization processes. First, metal thinning over sidewalls resulting from underlying topography is eliminated. Proper application of the CMP process planarizes the step edges allowing uniform-thickness films to be deposited over the buried sidewalls. Second, the optical lithography tools used for the advanced deep-submicrometer processes have a very limited depth of focus (< 1 μm). CMP provides global planarization on the size scale of a wafer-stepper exposure field (2–5 cm), which greatly reduces the depth-of-focus demands placed on the photolithography process. This report describes the CMP process and discusses its unique capabilities in several applications at Lincoln Laboratory.

The CMP process, shown schematically in Figure 4-1, utilizes circular, orbital lapping motions. The wafer (100–200 mm in diameter) is held polished side down in a rotating carrier head. The carrier head is pressed against a polishing pad attached to a rotating platen. The carrier head can also oscillate along the radius of the platen during the polishing process. Polishing slurry is delivered to the center of the pad during the CMP process. This provides, in total, a dozen variables to control the process: carrier rpm, platen rpm, carrier oscillation stroke and frequency, polish pressure, polish temperature, pad texture and composition, slurry particle type, particle size, slurry pH, and slurry flow rate.

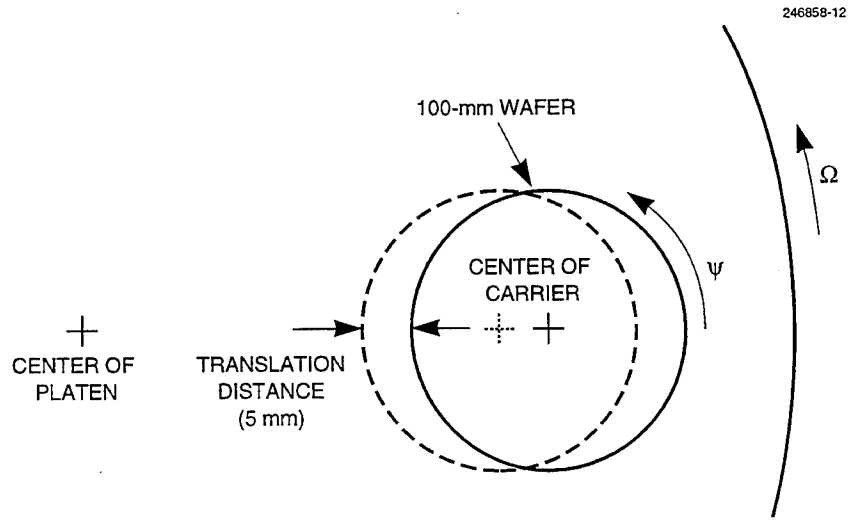

Figure 4-1. Schematic illustration of chemical mechanical polishing. The wafer is mounted in a rotating carrier and is pressed against a rotating polishing pad. The carrier moves back and forth across the pad to improve the uniformity.

The Westech model 372 CMP system used at Lincoln Laboratory provides an additional degree of freedom by allowing control of the radius of curvature of the wafer carrier head. A convex shape is generally used, which applies more pressure to the center of the wafer than to the edge. This induced wafer curvature is necessary to ensure good cross-wafer uniformity during the CMP process. The carrier and platen rpm are harmonically related to provide a uniform average surface velocity of pad and slurry across the wafer surface. However, during the polishing process, slurry is first delivered to the edge of the wafer, from which it works towards the wafer center. Slurry, like sandpaper, becomes less effective at removing material as it is used. Therefore, to offset the lack of "fresh" slurry at the wafer center the convex carrier head provides additional pressure to the wafer center to help balance the removal rate across the wafer surface.

Seven separate programs at Lincoln Laboratory depend on the CMP system. Two of these, back-side-illuminated ultraviolet (UV) and infrared (IR) imagers, utilize the system's traditional silicon polishing capabilities. To maximize the "fill factor" and to enhance the quantum efficiency of these devices, it is necessary to illuminate the imagers from the back side. Standard silicon processing starts with substrates that have intentional wafer back side damage, which helps to getter impurities that can impact device performance. During processing the back sides are coated with a variety of thin films and chemicals. However, for successful back side illumination it is important to produce a high-quality surface on the back side. For both of these imager programs the CMP system is used after device fabrication to produce a defect-free silicon surface on the wafer back side. This reduces the thickness of the 550-μm wafer by 25–50 μm. The CMP process is generally followed by a controlled wet-chemical etch to reduce the active wafer thickness to as thin as 10 μm.

The CMP system is also used to planarize intermetal dielectrics for multilevel metallization. Plasma-enhanced chemical vapor deposition (PECVD) tetraethylorthosilicate (TEOS) oxide films are planarized in the CMP system using a basic slurry (10.3 pH) containing colloidal silica particles. Individual slurry particle diameters range between 30 and 50 nm, but the particles tend to cluster together in groups of approximately 100 particles. PECVD TEOS interlevel dielectric oxides are planarized for both a two-level metal multichip module program and a low-power, 0.5-μm complementary metal oxide semiconductor process.

Two novel uses for CMP have been developed. One of these is the formation of self-aligned contacts to the top of silicon pillars in a vertical metal oxide semiconductor field-effect transistor (MOSFET) array used for a dense memory application. The other is the planarization of photoresist to alleviate the limited depth of focus inherent in deep-UV lithography.

The vertical MOSFET [2] structure shown in Figure 4-2 combines long-channel device characteristics with a submicrometer array pitch. The silicon substrate provides the source contact for all transistors in the array. The polysilicon gate and gate oxide encircle the structure, and drain contacts are formed on the tops of the cylindrical devices. Fabrication challenges include etching the structures, planarizing after gate fabrication, aligning the drain contacts, and preventing shorts between the gate and drain contacts. Two CMP steps are critically important to meeting these challenges. After the polysilicon gate has been deposited, CMP with a KOH and water slurry is used to remove the photoresist from the top of the silicon pillar prior to the polysilicon etch. This allows the polysilicon to be removed from the top of the silicon pillar and recessed down the sidewall during the etch, thereby preventing short circuits. After low-pressure chemical vapor deposition of a TEOS-based oxide, polishing with colloidal silica slurry is used to planarize the substrate and to allow the formation of self-aligned contacts to the drain regions on top of the silicon pillar. Functional devices with

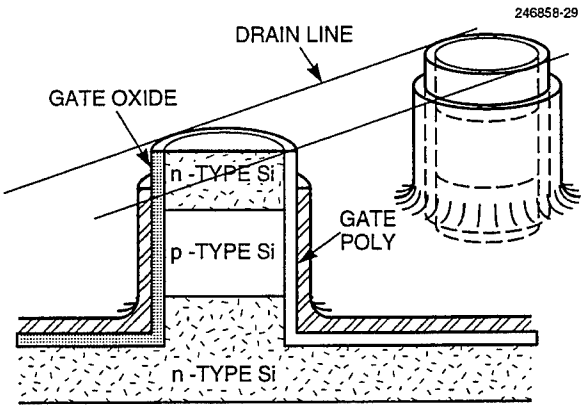

Figure 4-2. Cross-sectional diagram of vertical metal oxide semiconductor field-effect transistor (MOSFET) structure. The channel length is set by the height of the silicon cylinder, and the array pitch is set by the diameter. Thus, it is possible to achieve long-channel device performance in a densely packed array.

diameters down to 0.3 μm have been fabricated and contacted using CMP. This same technique is used in the fabrication of superconducting Josephson junctions, where instead of a silicon pillar a niobium/aluminum-oxide/niobium trilayer is used.

The CMP process has also been used to planarize hard-baked photoresist, which serves as an underlying organic layer in a 193-nm lithography bilayer resist process. The top photosensitive layer is a 30–50-nm-thick silicon-containing polymer film [3]. It is exposed with 193-nm illumination, developed in toluene, and then the pattern is transferred into the planarized layer using O_2 reactive ion etching. This planarized resist process helps to compensate for the limited depth of focus inherent in deep-UV exposure tools. Figure 4-3 shows the effectiveness of this process for metal definition in a simple planar MOSFET device. Initial, post-resist-coat, and post-CMP surface profiles for the gate contact region are shown.

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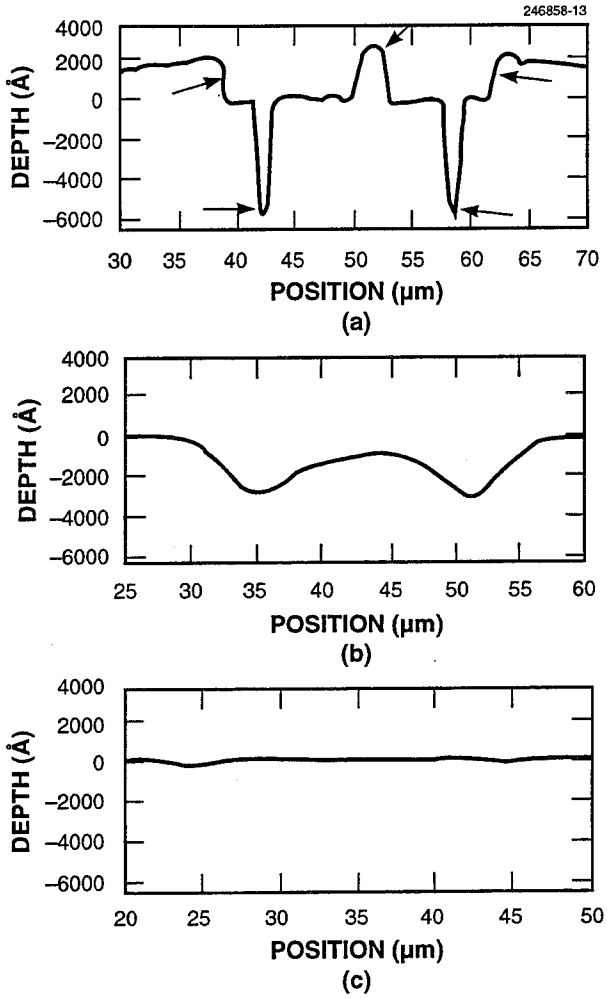

Figure 4-3. Surface profilometer traces showing effectiveness of chemical mechanical polishing (CMP) as part of bilayer resist process for MOSFET metal definition. (a) The nonplanar initial surface through a transistor active area showing from left to right (arrows) the field oxide to active area step, source/drain contact cut, gate step, source/drain contact cut, and field oxide step. (b) A layer of SPR-511 photoresist is deposited and hardbaked to partially planarize the surface. (c) CMP is used to fully planarize the surface. The photoactive layer is then applied.

4.2 DRY DEVELOPMENT FOR 193-nm SILYLATION RESIST

Single-layer resists have been widely used in optical photolithography, but as the resolution requirements approach 0.25 μm and below, advanced techniques such as top-surface imaging may become necessary. Top-surface imaging is insensitive to underlying topography and provides increased focus latitude [4]. Silylation, the incorporation of silicon in a polymer film, forms the basis for a top-surface imaging system developed at Lincoln Laboratory for use in 193-nm lithography [5]. This scheme requires dry development, that is, the anisotropic transfer of the surface image pattern through the resist layer. In order for this dry etch process to be commercially viable, a dry etch tool with high throughput and good uniformity is required. This report presents results on dry development of a 193-nm silylation resist in an oxygen-based plasma using a helicon high-ion-density plasma etcher.

The positive-tone 193-nm silylation resist process is illustrated schematically in Figure 4-4. An ~ 1-μm-thick polyvinylphenol (PVP) resin is selectively crosslinked by exposure in a 193-nm optical lithography system. The sample is then treated with a silicon-containing vapor (dimethylsilyldimethylamine) at a temperature of 90°C and a pressure of 25 Torr for 60 s. The uncrosslinked PVP areas incorporate a controlled

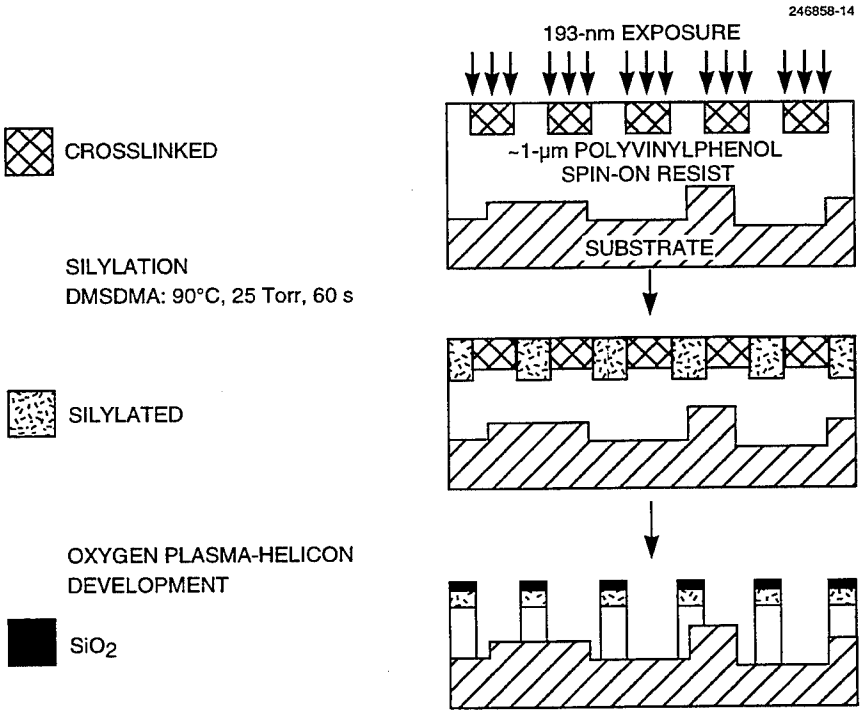

Figure 4-4. Schematic process flow for 193-nm, top-surface imaging, positive-tone silylation process. Exposure to 193-nm radiation results in selective crosslinking of the polyvinylphenol resin. The unexposed regions are then silylated in a dimethylsilyldimethylamine ambient. Finally, oxygen plasma converts the silicon to SiO_2, which masks the etching of the underlying resin.

amount of silicon, whereas the crosslinked areas do not. The wafers are then dry developed in an oxygen-based plasma. The oxygen reacts with the silylated areas to form SiO_2, which acts as a mask that protects the underlying resin. The unprotected resin areas are etched away by the oxygen plasma, thereby transferring the pattern. A complete optimization of the silylation resist scheme requires consideration of the exposure, silylation, and dry development steps, but in this study we have just focused on optimization of the dry development. The goal was to produce vertical resist profiles for 0.25-μm-wide features while maintaining good process latitude, high throughput, good uniformity, and linearity between different feature types.

In these experiments, unpatterned wafers consisting of ~ 1 μm of PVP with a 100-nm-thick silylated layer were used to optimize the effect of process conditions (source power, chuck power, O_2 flow rate, temperature, and pressure) to obtain etch rates > 1 μm/min, selectivity between the silylated layer and resist layer of > 20:1, and nonuniformity < 3%. Unless otherwise stated, the experiments summarized below used the following standard conditions: 2-kW source power, 50-W chuck power, 100-sccm O_2 flow rate, 0°C temperature, and 2-mTorr pressure. Figures 4-5–4-7 show the dependence of etch rate and selectivity on source power, chuck power, and flow rate. As expected, etch rate increases with increasing source power and chuck power. The rate also increases with flow rate, indicating the highly chemical nature of the dry development step. In another set of experiments, conducted with 75 W of chuck power, it was determined that

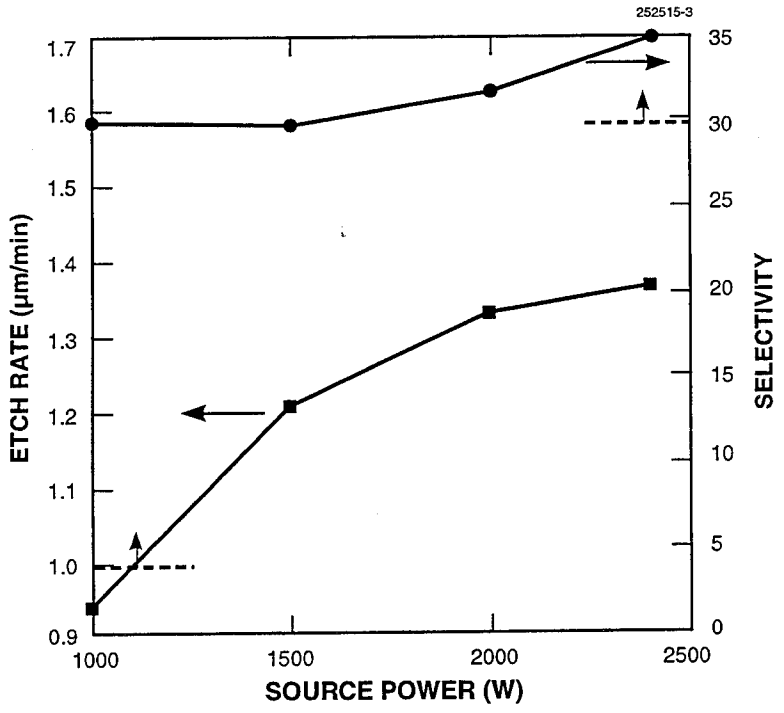

Figure 4-5. Dependence of etch rate and selectivity on source power under the standard conditions: 50-W chuck power, 100-sccm O_2 flow rate, 0°C temperature, and 2-mTorr pressure. Selectivity is defined as the ratio of the etch rate of the unsilylated resist to the etch rate of the silylated resist.

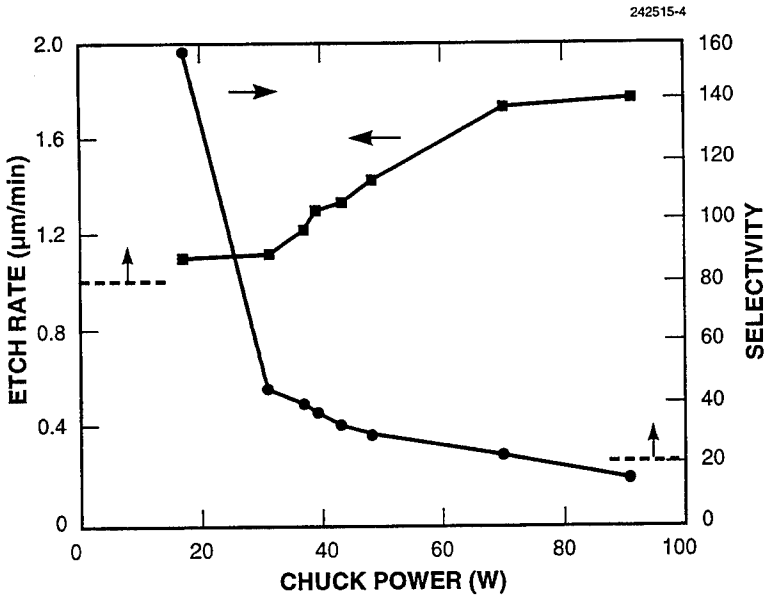

Figure 4-6. Dependence of etch rate and selectivity on chuck power, under standard conditions as in Figure 4-5.

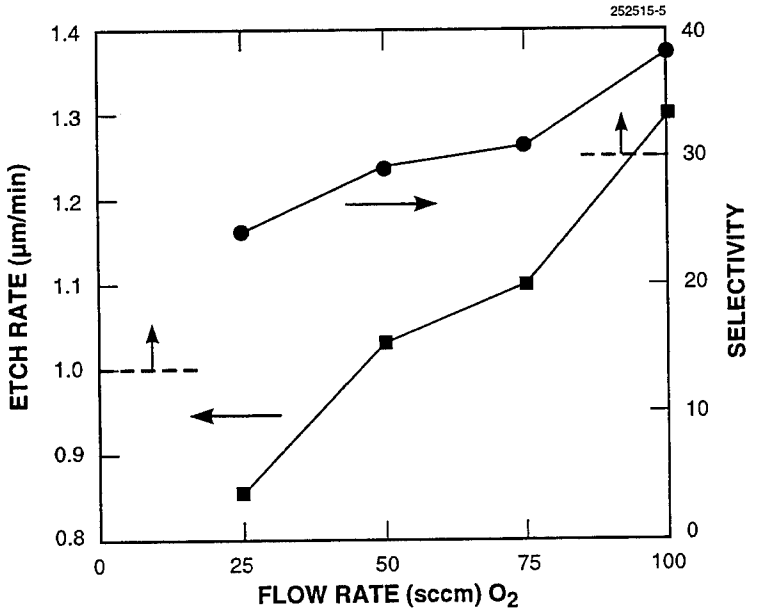

Figure 4-7. Dependence of etch rate and selectivity on flow rate, under standard conditions as in Figure 4-5.

reducing the chuck temperature from 25 to −100°C increases the etch rate from 1.4 to 1.6 μm/min. The etch rate is nearly independent of pressure between 1 and 6 mTorr. To achieve lower pressures the flow rate had to be decreased to 50 sccm, and these experiments indicated that from 1 to 0.5 mTorr the etch rate decreases from 1.05 to 0.90 μm/min. Our results also indicate that the etch rate varies with the amount of material being removed, consistent with results reported by Jurgensen et al. [6]. We found that under identical plasma conditions, the etch rate for 45-, 79-, and 180-cm^2 (3-, 4-, and 6-in.) wafers was 1.65, 1.35, and 1.05 μm/min, respectively. Under typical operating conditions etch rates > 1 μm/min are obtained on 100-mm wafers. This is sufficient to satisfy commercial throughput requirements.

Selectivity between the silylated and unsilylated resist is the variable that most dramatically affects exposure, focus, and etch process latitude as well as feature linearity. We have found that the chuck power is the etching parameter that produces the largest change in selectivity, as seen in Figure 4-6. Selectivity is nearly independent of pressure (1–6 mTorr) and temperature (25 to −100°C) at 2-kW source power, 50–75-W chuck power, and 100-sccm O_2. Again, we note a change at low pressure where the selectivity decreases from 30:1 at 2 mTorr to 20:1 at 0.5 mTorr, all other variables remaining the same. The selectivity at a given chuck power can be improved by increasing flow rate or source power. To obtain acceptable linewidth control with the 193-nm silylation resist, modeling indicates that one should have a selectivity > 20:1. For the conditions in Figure 4-6, this requirement is satisfied when the chuck power is < 75 W. However, in order to avoid the formation of residue in the etched areas the chuck power must be > 25 W. These constraints dictate an operating window for chuck power of 35–75 W. Under these optimized process conditions, blanket wafer etch rate nonuniformity is less than ± 3% over 85 mm of a 100-mm wafer.

In addition to adequate selectivity, it is necessary to optimize the resist profile. We have observed an isotropic etching component, sidewall bowing, and aspect-ratio-dependent etching. Improvement in anisotropy and linewidth control is obtained by increasing chuck power and decreasing temperature. For example, at low chuck power (35 W) there is a significant isotropic etching rate, whereas at 75 W the isotropic etch rate is drastically reduced. We also have found that decreasing the chuck temperature from 0 to −100°C eliminated the isotropic etching component.

Patterned silylation wafers were etched to evaluate pattern transfer into resist and process latitude for the silylation process. Figure 4-8 is a scanning electron micrograph of 0.20-μm equal line-and-space gratings etched at 2-kW source power, 75-W chuck power, 100-sccm O_2 flow rate, −100°C temperature, and 2-mTorr pressure. These were the etch conditions determined to be optimum from the above experiments. The vertical etch rate under these conditions was 1.4 μm/min at a selectivity of 27:1, and linearity (± 10%) was maintained for isolated lines, spaces, and equal line-and-space gratings for a 25% (exposure dose 100 mJ/cm^2) and a 100% (exposure dose 110 mJ/cm^2) overetch. Total exposure latitude vs feature size (equal line-and-space gratings) is shown in Figure 4-9. The total exposure latitude for 0.35-μm equal line-and-space gratings is 54% for this process at 193 nm, double that obtained recently for a 248-nm silylation resist [7]. Focus latitude for the 0.20-μm features is 1.2 μm.

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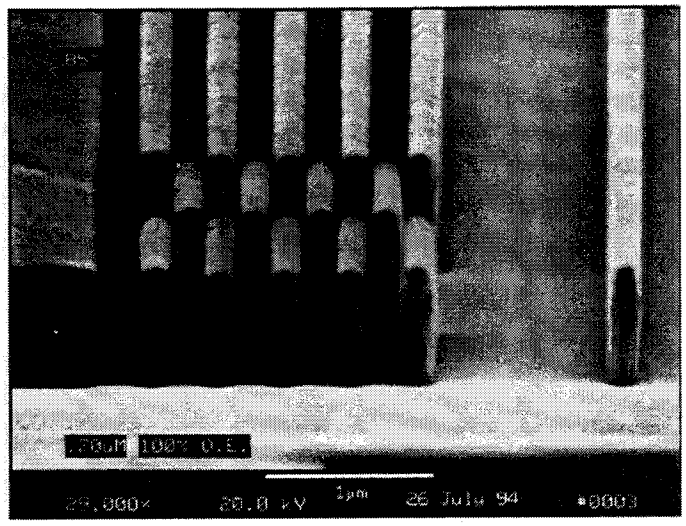

Figure 4-8. Scanning electron micrograph of 0.20-μm features etched at 2-kW source power, 75-W chuck power, 100-sccm O_2 flow rate, –100°C temperature, and 2-mTorr pressure (100% overetch) and silylated at 90°C and 25-Torr pressure for 60 s.

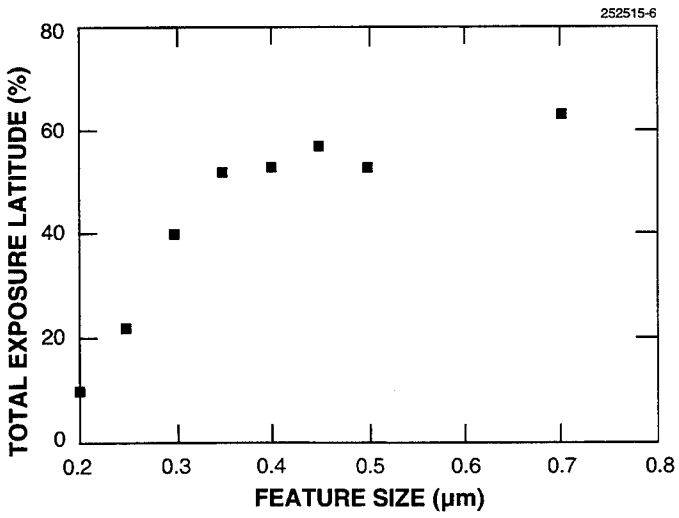

Figure 4-9. Total exposure latitude for equal line-and-space gratings for features with vertical profiles (± 10% linearity) and silylated at 90°C and 25 Torr for 60 s.

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5. HIGH SPEED ELECTRONICS

5.1 EFFECT OF SPACE CHARGE ON VACUUM MICROTRIODE RF PERFORMANCE

Space charge plays an important role in thermionic vacuum tubes, but it has often been neglected in modeling field-emitter cathodes. To realize useful power gain at frequencies above 10 GHz, field-emission microtriodes require high transconductance g_m for a given current level (high g_m/I ratio) [1] as well as high current densities. Higher g_m/I ratios can be achieved by reducing the emitter-tip radius, reducing the tip-to-gate spacing, and/or using emitter materials having low work function. However, these changes also result in lower electric fields in the devices, which reduce the current-density threshold at which space charge effects begin to limit the transconductance and gain. We have simulated these deleterious effects numerically in order to develop criteria that will minimize them.

The software program EGUN2 was used to determine solutions to Poisson's equation and provide particle trajectories for simulations of the standard gated-cone arrays fabricated at Lincoln Laboratory. The geometry of these arrays is shown in Figure 5-1. EGUN2 can calculate the current in the device using either a Fowler-Nordheim or a Child's law formalism. In our work these two solutions were merged to determine the full current-voltage characteristics for an array like that of Figure 5-1(b), as shown in Figure 5-2 with work function ϕ as a parameter. The solid lines depict Fowler-Nordheim emission with space-charge effects neglected, and the dashed curves represent emission with space charge taken into account. For the low work functions of 0.5 and 1.0 V, the electron beam emitted from each cone does not diverge appreciably as it approaches the anode, and the current is limited by the space charge in that beam only. For the higher work functions, the higher gate voltages cause the electron beams to flare substantially, so that beams from neighboring cones overlap as they approach the anode. The space-charge-limited (SCL) current in this case is governed by effects in the overlapping beams and is lower than that expected by considering the space charge in only one flared beam.

The dotted line in Figure 5-2 is a locus of constant unity-current-gain frequency f_T calculated using the Fowler-Nordheim characteristics. A comparison of this line with the SCL current clearly shows that f_T values > 100 GHz can be reached for low values of ϕ, whereas f_T will be limited to lower frequencies at higher values of ϕ. Increasing the cone-to-cone spacing for arrays with higher work functions will not improve the f_T significantly for this case, however, because the relative proportion of parasitic gate-to-substrate capacitance is also increased. Alternatively, increasing the packaging density of an array improves the current, f_T, and g_m, but sharper cones, reduced tip-to-gate spacing, and/or reduced ϕ must be produced concomitantly in order to avoid space-charge effects.

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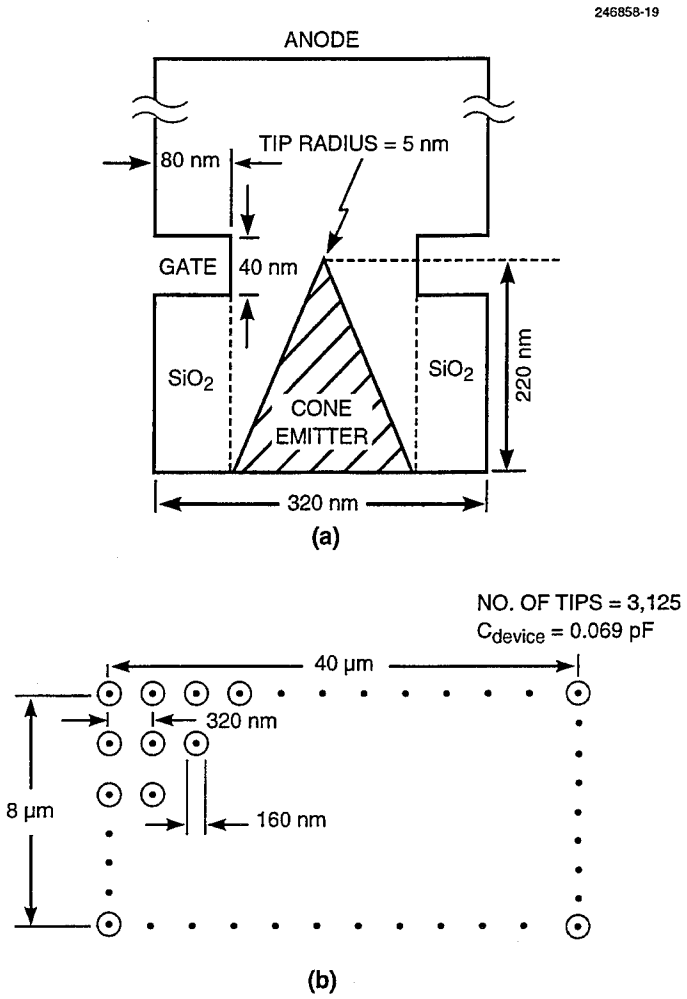

Figure 5-1. Microtriode geometry used in simulations: (a) unit cell and (b) top view of geometry of our high-density cone array.

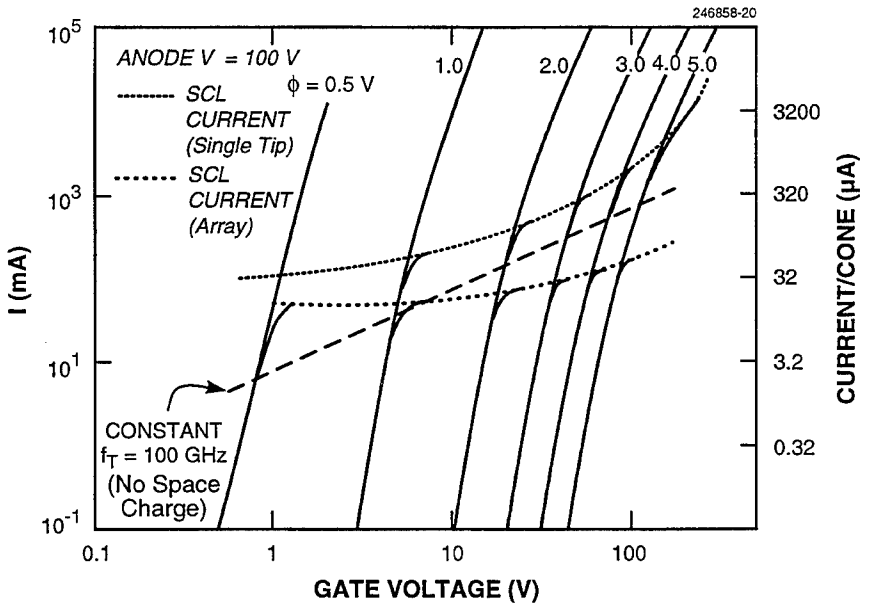

Figure 5-2. Array current for geometry of Figure 5-1 for a range of work functions ϕ from 0.5 to 5.0 V. At low currents the anode current is due to field emission (solid curves), and at higher currents becomes space-charge limited (dotted curves). Shown for reference is a dashed locus of constant f_T calculated using the Fowler-Nordheim curves.

6. MICROELECTRONICS

6.1 ELECTRON TRAPPING AT DISLOCATIONS IN A BURIED-CHANNEL CHARGE-COUPLED DEVICE

A previous report [1] described the effects of dislocations in charge-coupled device (CCD) imagers made on high-resistivity float-zone silicon wafers for soft-x-ray detection. The dislocations are formed as the result of plastic deformation of the wafers during high-temperature process steps and manifest themselves as bright defects (pixels with higher dark current) in video images. We have observed that devices with large numbers of such defects also have elevated charge-transfer inefficiency, suggesting that the dislocations can, in addition, trap electrons. Both effects are deleterious to the performance of devices that must operate at low signal levels, such as soft-x-ray sensors operating in a combined imaging/spectroscopic mode. We describe here measurements that enable us to determine both the trapping properties of the dislocations and their location at a specific gate within a pixel.

For this study we used a technique originally described by Lemonier and Piaget [2] to reveal the location of defects that cause charge loss, and we added features to enable determination of the trap time constants. Figure 6-1 describes this method for the case of a three-phase CCD with empty trap levels under phases 2 and 3. Phase 1 is set to a high level, and the wells are partially filled with charge. If the charge is clocked to the right by two gates, both traps will be filled and the packet will have a net deficit of two electrons. The packets are then immediately clocked back to their original position, and the clocks are held stationary for a time t_w. If t_w is sufficiently long the traps will empty, and the electron in the phase 2 trap will rejoin its parent packet while the phase 3 electron will join the packet on the right. Note that if there are traps under the phase 1 gates they will have no effect, as they will be immediately filled at the beginning and remain so during the clocking sequence. If this forward-reverse-wait process is repeated M times, then the left and right wells will have a deficit and a surplus, respectively, of M electrons, solely as a result of the phase 3 trap. Therefore, as this example has shown, the technique can locate a trap to within a particular phase. If the same sequence is used but with phase 3 as the storage well, then traps under phase 2 will be revealed.

The characteristic emission time τ_e can be obtained by varying t_w and measuring the charge deficit or surplus in the two wells. The probability that a trap, filled at $t = 0$, will empty by time $t = t_w$ is $1-\exp(-t_w/\tau_e)$. If there are N_t traps under a gate, then the charge surplus or deficit Δn is

$$\Delta n = \pm M N_t \left[1 - \exp\left(-t_w/\tau_e\right)\right] . \tag{6.1}$$

From the Shockley-Read-Hall theory, the emission time τ_e is related to the trap energy E_t and capture cross section σ by

$$1/\tau_e = \sigma v_{\text{th}} N_c \exp\left[-(E_c - E_t)/kT\right] , \tag{6.2}$$

where v_{th} is the electron thermal velocity, N_c is the conduction band density of states, E_c is the conduction band energy, and T the temperature.

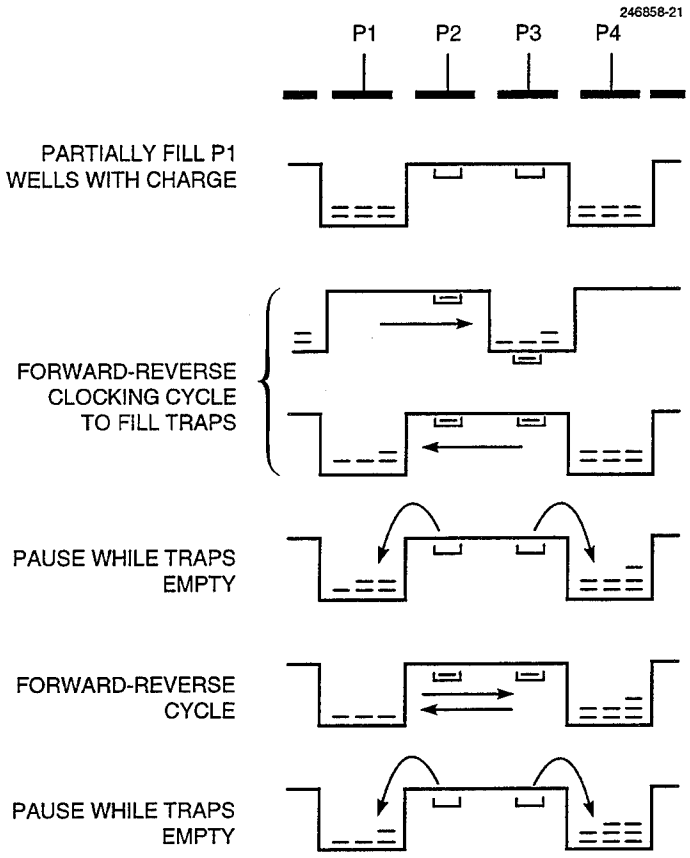

Figure 6-1. Technique employed to measure properties of trap levels in a charge-coupled device.

We have used this technique to clock CCDs with known high concentrations of dislocations. The devices are 420×420-pixel frame-transfer devices fabricated on 5500-Ω cm, *p*-type float-zone silicon wafers. The video images from such devices show the expected bright/dark pixel pairs, and in many cases they form lines lying parallel to the rows and columns of the imager as in the case of the dislocation arrays revealed by etching [1]. Video images of defects shown by this CCD technique have been compared to the same sample after preferential etching to reveal dislocations. In most cases we find etch pits in the same pixel location as revealed by the multi-reversal clocking technique. This provides further evidence linking the charge-transfer loss to the presence of the dislocations. Figure 6-2 shows a plot of Δn for two adjacent pixels as a function of wait time t_w at three temperatures. For this experiment the device was illuminated by a pulsed light-emitting diode to fill the wells with ~ 12 000 e^-, and then cycled 500 times before being read out. The solid curves are the result of fitting Equation (6.1) to the data, and from this fit we obtain both τ_e and N_t. By inspection of Figure 6-2 we can see that $N_t \approx 6000/500$ or 12, implying that the dislocation has 12 trap sites along the portion of its length that lies in the CCD channel. For the device studied here the values of N_t range from 1 to 20. Figure 6-3 is an Arrhenius plot of the emission time-constant data, from which we find that $E_c - E_t = 0.33$ eV and

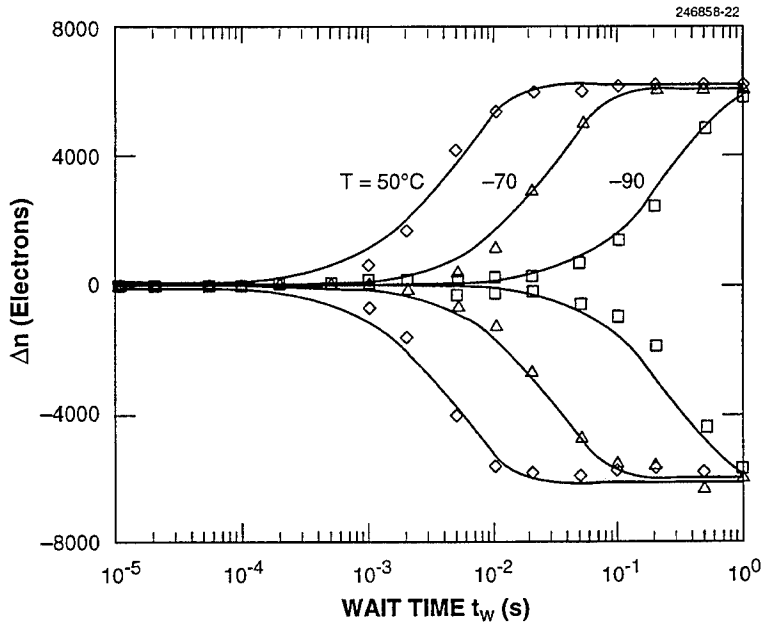

Figure 6-2. Measurements of charge deficit and surplus in adjacent pixels as function of wait time t_w at three temperatures. The solid lines are the best fit of the data to a theoretical expression.

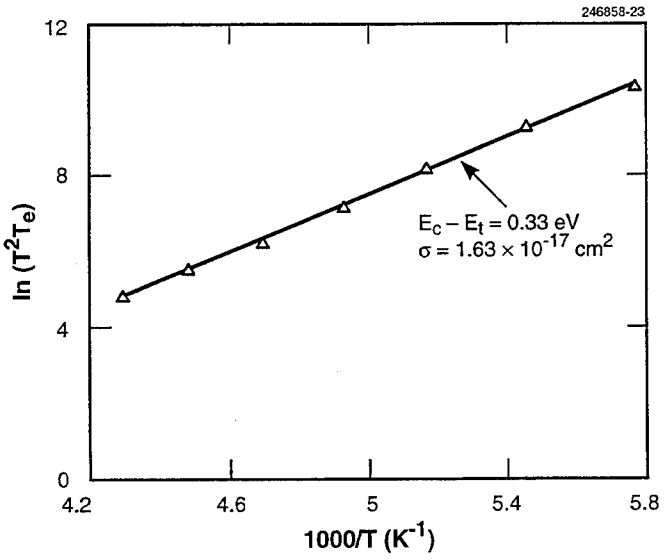

Figure 6-3. Arrhenius plot of trap emission time data.

$\sigma = 1.63 \times 10^{-17}$ cm^2. These values agree quite well with those determined by deep-level transient spectroscopy on intentionally deformed Si, where $E_c - E_t = 0.38$ eV [3],[4].

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7. ANALOG DEVICE TECHNOLOGY

7.1 FERRITE-SUPERCONDUCTOR MICROWAVE PHASE SHIFTERS

A major source of losses in conventional ferrite devices, particularly in microstrip and stripline geometries, is the electrical resistance of the conductor circuits, which are usually copper or gold. Because superconductor surface resistances deteriorate in magnetic fields [1], however, the use of superconductors to solve the conduction loss problem has not been an attractive option. For designs where significant magnetic fields penetrate the circuit [2], superconductivity may have no advantage over copper at 77 K. Yet, the conduction losses may be reduced dramatically through the use of superconductors in conjunction with magnetic structures that confine the magnetic flux to the ferrite. This report describes the principle of operation and performance of experimental microwave ferrite phase shifters with superconducting microstrip circuits.

For optimum performance of devices comprising magnetized ferrites in proximity to superconductors, magnetic flux invasion of the superconductor must be minimized. This can be achieved with designs based on flux confinement within closed magnetic paths [3]. The essence of this concept is the confinement of dc magnetic flux within the ferrite, thereby avoiding external dc magnetic field penetration of the superconductor, while permitting RF magnetic field penetration of the ferrite.

To demonstrate more clearly the potential of this technology, two designs of nonreciprocal phase shifters were constructed with meanderline circuits that produce nonreciprocal phase shift when the magnetization is parallel to the meanders. The meanders are a quarter-wavelength long at the device center frequency, thereby creating circular polarization in the center of each meander [4]–[6]. To show the principle of operation, a thin film of Nb at 4.2 K was used for the superconductor. In the first phase shifter, shown in Figure 7-1, the Nb circuit was deposited directly on the ferrite (magnetization $4\pi M$ of 1200 G) to optimize the interaction between microwave signal and ferrite. The second phase shifter, shown in Figure 7-2, consisted of a Nb circuit deposited on a lanthanum aluminate ($LaAlO_3$) substrate, with the ferrite pressed onto the circuit.

The ferrite circuit takes the form of a rectangular toroid that completes the magnetic circuit and establishes the collinearity of the magnetization with the meanders. The magnetization reversal for the measurement of differential phase shift is accomplished through dc current switching in the magnetizing coil. As discussed below, the devices were operated both in the remanent state without current in the coil, and in saturation with current flowing in the coil.

Insertion loss for the device of Figure 7-1 is shown in Figure 7-3. The increased-loss regime at frequency $f < 5$ GHz was caused by the interaction between the microwave signal and the partially magnetized ferrite [7],[8] through ferrimagnetic resonance. Reflection losses recorded for these transmission measurements were generally in the range 10–15 dB, but were influenced by attenuation in the lengthy cabling required to access the Dewar enclosure. Subtraction of reflection losses revealed a device absorption loss < 0.3 dB between 6 and 12 GHz with differential phase shift for magnetic saturation increasing monotonically to 500° at 12 GHz, as seen in Figure 7-4, thereby producing an intrinsic figure of merit (FOM) > 1000°/dB over most of this frequency range. Adjustments to the circuit design are expected to move the phase shift maximum closer to the center of this band.

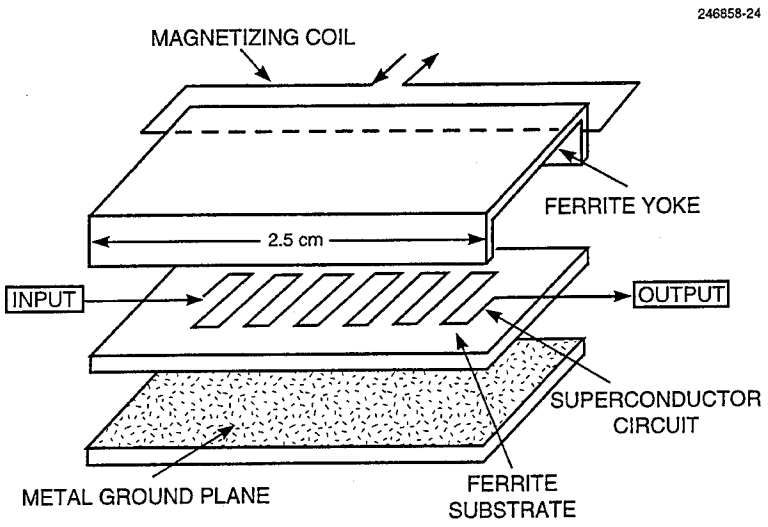

Figure 7-1. Experimental phase shifter with Nb meanderline superconductor direct deposited on ferrite. Magnetic flux is confined within the ferrite toroidal structure.

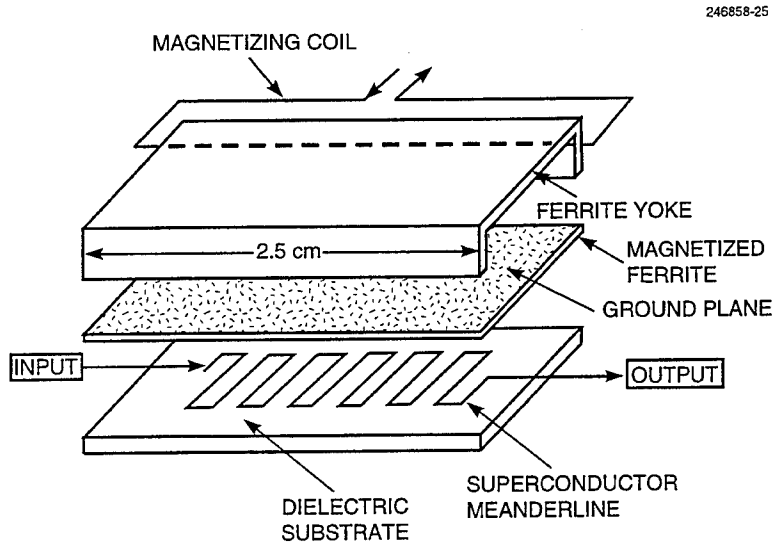

Figure 7-2. Experimental phase shifter with Nb meanderline superconductor deposited on dielectric and pressed in contact with ferrite. Magnetic flux is confined within the ferrite toroidal structure.

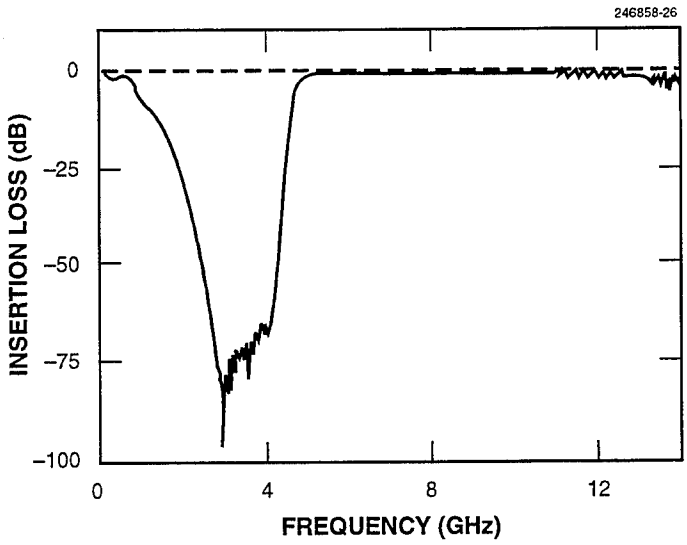

Figure 7-3. Insertion loss vs frequency of Nb meanderline superconductor-on-ferrite phase shifter, shown in Figure 7-1. The loss also included reflection effects from impedance mismatches.

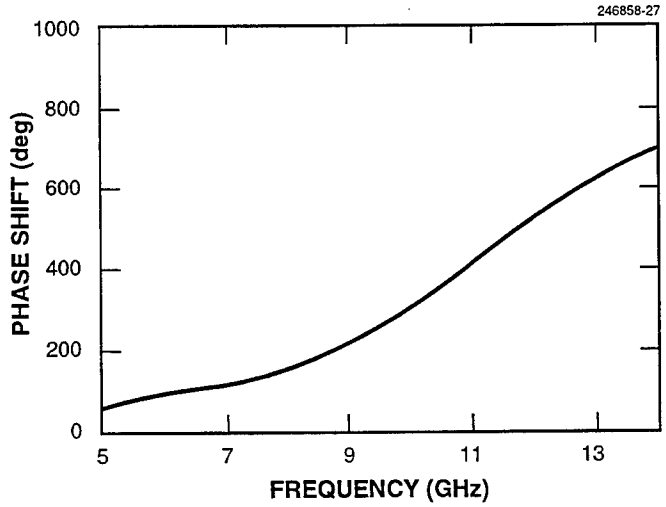

Figure 7-4. Differential phase shift vs frequency from Nb meanderline circuit on ferrite substrate, shown in Figure 7-1.

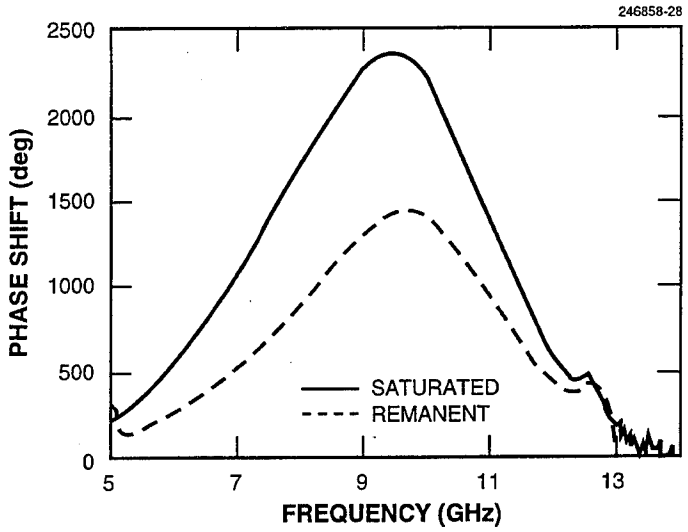

Figure 7-5. Differential phase shift vs frequency from Nb meanderline circuit on $LaAlO_3$ substrate, shown in Figure 7-2.

Figure 7-5 presents differential phase shift results for the device of Figure 7-2 with the same ferrite as the device of Figure 7-1 but with $LaAlO_3$ as the substrate. A peak phase shift of 2400° occurred at 9.5 GHz for the ferrite in the magnetically saturated state, and 1400° in the remanent state. The absorption loss after corrections for reflection losses was < 1 dB in the frequency range of interest. The difference in phase shift characteristics between the two device configurations is partly the result of the different dielectric environments of the superconductor circuits.

The FOM values obtained in these experiments may be compared with 130°/dB (value at remanence) at X-band reported by Roome [9] with a copper meanderline circuit at room temperature. If we estimate the surface resistance decrease of copper at 77 K, we may infer that the corresponding superconductor device would have fivefold higher FOM than a device using the best normal conductor. For an optimized design with ideal impedance matching of the superconductor circuit and full utilization of $4\pi M$, FOM values approaching 10 000°/dB could be anticipated.

On the basis of information derived from these experiments, a design that incorporates a high-T_c YBCO patterned film on an appropriate substrate will be adopted for a similar demonstration at $T = 77$ K, following the design shown in Figure 7-2. We expect that the results with YBCO at 77 K will be comparable to those of Nb at 4 K, and that FOMs substantially higher than presently possible with normal conductors in microstrip geometries or with conventional waveguide technology will soon be demonstrated at liquid-nitrogen temperatures. The magnetic flux confinement principle of this device concept should be applicable to any combination of magnetic and superconducting materials.

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